CLAIMS

1. (Corrected) A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit between a GND power source terminal (ground power source terminal) of the level conversion core circuit and a GND power source (ground power source), the switching circuit being controlled by a third logic circuit to produce a control signal under control of the first power source,

the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the switching circuit,

the level conversion core circuit including a p-MOS cross-coupled latch including at least two first p-MOS, a differential n-MOS including at least two n-MOS, and at least two second p-MOS,

the p-MOS cross-coupled latch including a source terminal connected to the second power source and a gate terminal connected to a level conversion output which is each drain terminal of a second p-MOS,

the differential n-MOS including each source terminal connected to the GND power source, each drain terminal connected to the level conversion output, and each gate terminal connected to a level conversion input,

the second p-MOS including each source terminal connected of the first p-MOS, each gate terminal connected to the level conversion input, and each drain terminal connected to the level conversion output.

2. (Corrected) A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a switching circuit between a power source terminal of a level conversion core circuit and the second power source, the switching circuit being controlled by a third logic circuit which generates a control signal under control of the first power source, and a pull-up and/or pull-down circuit at an output of the level conversion core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit,

the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

3. A level converting circuit in accordance with claim 1 or 2, characterized in that:

the level conversion core circuit includes a p-MOS cross-coupled latch including at least two p-MOS and a differential n-MOS including at least two n-MOS;

each of the p-MOS includes a source terminal connected to the second power source terminal and a gate terminal connected to a level conversion output which is each drain terminal; and

each of the n-MOS includes a source terminal connected to the cross-coupled latch and the GND power source terminal, a drain terminal connected to the level conversion output, and a gate terminal connected to a level conversion input.

4. (Deleted).

5. (Corrected) A level converting circuit for converting a signal level of a first logic circuit to which a first power source is

supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit which is disposed between a power source terminal of the level conversion core circuit and the second power source and which is controlled by a third logic circuit, the third logic circuit generating a control signal under control of a first power source, wherein the control circuit is controlled by a control signal from the third logic circuit.

6. A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit, a control circuit to which the second power source is supplied and which receives as inputs thereto a level conversion input signal and the level conversion output signal, and a switching circuit which is disposed between a power source terminal of the level conversion core circuit and the second power source and which is controlled by a third logic circuit, the third logic circuit generating a control signal under control of the first power source, wherein the control circuit is controlled by a control signal from the third logic circuit.

7. A level converting circuit, characterized in that the third logic circuit controls the control circuit by a control signal from the third logic circuit, and the control circuit produces control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

8. A level converting circuit in accordance with claim 7, characterized in that the control circuit further produces

a control signal to control the pull-up and/or pull-down circuit to thereby control the pull-up and/or pull-down circuit.

9. (Deleted).

10. (Corrected) A level converting circuit in accordance with claim 8, characterized in that the pull-up and/or pull-down circuit comprises a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal, and a drain terminal connected to one of the level conversion outputs and an n-MOS including a source terminal connected to a GND power source, a gate terminal connected to an inverted signal of a control signal, and a drain terminal connected to other one of the level conversion outputs.

11. (Corrected) A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other p-MOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; and additionally at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs.

12. (Corrected) A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, each drain terminal of other p-MOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; and additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, a drain terminal connected to one of the level conversion outputs.

13. (Corrected) A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level

conversion outputs.

14. (Corrected) A level converting circuit in accordance with claim 7, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs; at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs; and additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to one of the level conversion outputs.

15. (Corrected) A level converting circuit in accordance with claim 7, characterized in that the control circuit comprises a NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit and a NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit, wherein an output signal of the NAND circuit is produced as a control signal.

16. (Corrected) A level converting circuit in accordance with claim 15, characterized in that the NAND circuit is of a CMOS circuit

configuration and the p-MOS transistor to which the level conversion input signal is connected includes a transistor at least having a small ratio of a channel width/a channel length or a high threshold value.

17. (Corrected) A level converting circuit in accordance with claim 15, characterized in that the NAND circuit is of a CMOS circuit configuration and the n-MOS transistor to which a control signal output of the third logic circuit is connected includes a source terminal connected to a GND power source.

18. (Deleted).

19. A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs; and additionally at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the third logic circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs.

20. A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit further includes at least two p-MOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs; and additionally a p-MOS including a source terminal connected to the second power source, a

gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs.

21. A level converting circuit in accordance with claim 15, characterized in that the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to each of the level conversion outputs; additionally a p-MOS including a source terminal connected to the second power source, a gate terminal connected to a control signal from the third logic circuit, and a drain terminal connected to one of the level conversion outputs; and

additionally an n-MOS including a source terminal connected to the GND power source, a gate terminal connected to a control signal from the third logic circuit or to an inverted signal of the control signal, and a drain terminal connected to other one of the level conversion outputs.

a control signal.

47. A level converting circuit in accordance with claim 38, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the OR-NAND circuits is produced as a control signal.

48. (Corrected) A level converting circuit in accordance with claim 47, characterized in that the level conversion core circuit comprises a p-MOS cross-coupled latch including at least two of the p-MOS in which each source terminal is connected to the second source and a gate terminal of other p-MOS is connected to each of the level conversion outputs, at least two p-MOS switches including a source terminal connected to a drain terminal of the p-MOS, each gate terminal connected to a control signal from the control circuit, and each drain terminal connected to the level conversion outputs, and a differential n-MOS switch including at least two n-MOS each of which includes a source terminal connected to a GND power source, a drain terminal connected to the respective level conversion outputs, and a gate terminal connected to a level conversion input.

49. (Corrected) A level converting circuit in accordance with one of claims 11 to 14, 19 to 22, and 24 to 27, characterized in that the control circuit comprises a first NAND circuit to which the second

power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit, a second NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective NAND circuits, wherein each output signal from the first and second NAND circuits and the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal of the inverters is produced as a control signal of the level conversion core circuit.

50. (Corrected) A level converting circuit in accordance with one of claims 11 to 14, 19 to 22, and 24 to 27 characterized in that the control circuit comprises a NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, a NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which respectively receive as inputs thereto outputs from the respective NOR circuits, wherein each output signal from the NOR circuits and the inverters is produced as a pull-up and/or pull-down control signal and each output signal of the NOR circuits is produced as a control

signal of the level conversion core circuit.

51. (Deleted)

characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit, a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the first and second OR-NAND circuits, wherein each output signal from the at least two inverters is produced as a pull-up and/or pull-down control signal and each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-up and/or pull-down circuit includes at least two p-MOS each of which includes a source terminal connected to the second power source and a gate terminal connected to a control signal from the control circuit, a drain terminal of other p-MOS being connected to each of the level conversion outputs.

56. (Corrected) A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output, and a control output of

the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal from the inverters is produced as a pull-up and/or pull-down control signal, each output signal from the inverters is produced as a control signal of the level conversion core circuit, and

the pull-up and/or pull-down circuit includes at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

57. (Corrected) A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-up and/or pull-down circuit includes at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

58. (Corrected) A level converting circuit in accordance with one of claims 5 to 8, characterized in that the control circuit comprises an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output signal, and a control output of the third logic circuit or an inverted signal of the control output, an AND-NOR circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, and at least two inverters to which the second power source is supplied and which receive as inputs thereto outputs from the respective AND-NOR circuits, wherein each output signal of the inverters is produced as a control signal of the level conversion core circuit.

59. (Corrected) A level converting circuit in accordance with one of claims 4 to 7 and 9 to 11, characterized in that the control circuit comprises an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and an OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit.

60. (Corrected) A level converting circuit in accordance with one of claims 1, 3, 8, 58 and 59, characterized in that:

the level conversion core circuit comprises a p-MOS cross-coupled latch including at least two first p-MOS, a differential n-MOS including at least two n-MOS, and at least two second p-MOS, wherein:

the p-MOS cross-coupled latch includes a source terminal connected to the second power source and a gate terminal connected to a level conversion output which is each drain terminal of the second p-MOS;

the differential n-MOS includes each source terminal connected to the GND power source, each drain terminal connected to the level conversion output, and each gate terminal connected to a level conversion input; and

the second p-MOS includes each source terminal connected of the first p-MOS, each gate terminal connected to the level conversion input, and each drain terminal connected to the level conversion output.

61. A level converting circuit for converting a signal level of a first logic circuit to which a first power source is supplied into a signal level of a second logic circuit to which a second power source is supplied, characterized by including

a pull-down circuit at a level conversion output of a level conversion core circuit and a control circuit to which the second power source is supplied and which receives as inputs thereto a level conversion input signal and the level conversion output signal to produce control signals for a pull-down circuit and a level conversion core circuit, wherein the control circuit is also connected to control signals from the third logic circuit.

62. A level converting circuit in accordance with claim 61, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the second power source is supplied

and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core circuit, and

the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

63. A level converting circuit in accordance with claim 61, characterized in that the control circuit, the control circuit comprises a first OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto an inverted signal of the level conversion input signal, a positively inverted signal of the level conversion output signal, and a control output of the third logic circuit and a second OR-NAND circuit to which the second power source is supplied and which receives as inputs thereto a positively inverted signal of the level conversion input signal, an inverted signal of the level conversion output, and a control output of the third logic circuit or an inverted signal of the control output, wherein each output signal from the first and second OR-NAND circuits is produced as a pull-up and/or pull-down control signal, each output signal from the OR-NAND circuits is produced as a control signal of the level conversion core

circuit, and

the pull-down circuit, the pull-up and/or pull-down circuit include at least two n-MOS each of which includes a source terminal connected to the GND power source, a gate terminal connected to a control signal from the control circuit, and a drain terminal connected to the level conversion outputs.

64. (Deleted).

cross-coupled latch of the level converting circuit and hence the gate terminal of the n-MOS possibly exceeds a threshold value of the n-MOS.

In this case, since a conduction path appears between the second power source and a GND power source, there occurs a problem that a feedthrough current flows.

Additionally, in a case in which the first power source turns on and an input signal is inverted in a hold state, there exits a problem that the power source level increases to a predetermined level and the feedthrough current flows until the level conversion output is completely changed.

Moreover, the additional n-MOS has a function to enhance the function of the level converter circuit to hold the state of the p-MOS cross-coupled latch. Therefore, the level conversion delay increases, particularly, when the potential difference between the first and second power sources becomes large; the level conversion margin is lost and hence the level conversion cannot be conducted. That is, there also occurs a problem that even the input signal changes, the desired output cannot change.

It is a first object of the present invention to provide a level converting circuit in which occurrence of the feedthrough current can be suppressed even when the first power source is controlled and the increase in delay can also be suppressed in the level conversion.

DISCLOSURE OF THE INVENTION

Inventions of a level converting circuit in accordance with the present invention are a group of level converting circuits each of which includes a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit between a GND power source terminal (ground power source terminal) of the level

conversion core circuit and a GND power source (ground power source), the switching circuit being controlled by a third logic circuit to produce a control signal under control of the first power source, the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the switching circuit. In accordance with the present invention, it is also possible that there are arranged a switching circuit between a ground power source terminal of a level conversion core circuit and a second power source, the switching circuit being controlled by a third logic circuit which generates a control signal under control of a first power source and a pull-up and/or pull-down circuit at an output of the level conversion core circuit, the pull-up and/or pull-down circuit being controlled by the third logic circuit, the third logic circuit producing control signals to control the pull-up and/or pull-down circuit and the level conversion core circuit.

It is favorable that the level conversion core circuit includes a p-MOS cross-coupled latch including at least two p-MOS and a differential n-MOS including at least two n-MOS, wherein the p-MOS includes a source terminal connected to the second power source and a gate terminal connected to a level conversion output which is each drain terminal and the n-MOS includes each source terminal connected to the GND power source terminal, each drain terminal connected to the level conversion output, and each gate terminal connected to a level conversion input.

In accordance with the present invention, it is also possible that there are included a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit and a switching circuit between a power source terminal of the level conversion core circuit and a second power source, the switching circuit being controlled by a third logic circuit to produce a control signal under control of the first power

source, the control circuit being controlled by a control signal from the third logic circuit.

In accordance with the present invention, it is also possible to adopt a configuration including a pull-up and/or pull-down circuit in which the second power source is supplied to a level conversion output of a level conversion core circuit, a control circuit to which the second power source is supplied and which receives as inputs thereto a level conversion input signal and a level conversion output signal, and a switching circuit between a power source terminal of the level conversion core circuit and a second power source, the switching circuit being controlled by a third logic circuit to produce a control signal under control of the first power source, the control circuit being controlled by a control signal from the third logic circuit.